UNIVERSITY OF NORTH CAROLINA AT CHARLOTTE
Department of Electrical and Computer Engineering

EXPERIMENT 1 – INTRODUCTION TO THE EMONA SIGEX BOARD FOR NI ELVIS

OBJECTIVES
The purpose of this experiment is to familiarize the student with the various instruments and functions available on the SIGEx board and how they are used.

MATERIALS/EQUIPMENT NEEDED
NI ELVIS II
EMONA SIGEx Signal & Systems add-on board
Assorted patch leads
Two BNC – 2mm leads

INTRODUCTION
The experiments possible with the EMONA SIGEx board bring together mathematical theory and practical implementation of signals and systems. Students are able to explore, in a hands-on manner, the representation of physical processes by mathematical models and test and measure the benefits and limitations of such models. Through measurements, calculations and observations the aim is to consolidate understanding of signals and systems.

The SIGEx board customizes the instrumentation available on the NI ELVIS to create experiment-specific instruments which can be used to create many different circuit structures. As well, the ability to programmatically control, measure and automate measurements using LabVIEW bring students closer to real-world practices of system control and monitoring.

By implementing the many mathematical model and theorems in real hands-on circuit based experiments, the student reinforces and actualizes their understanding of these principles to create a solid foundation for future learning. Another important skill for engineers is the ability to take rigorous and precise measurements, often repetitively, in order to study the phenomena at hand. The EMONA SIGEx Signals & Systems Experimenter provides an abundance of opportunities to learn and practice experimental methodology in a variety of topics related to signals and systems.

EMONA SIGEX BOARD OVERVIEW
The SIGEx board is a collection of independent circuit blocks which each implement a single simple function. No one block is a complete experiment, however several blocks together can implement a wide variety of different experiments. The block inputs and outputs are patched together with 2 mm patching leads.

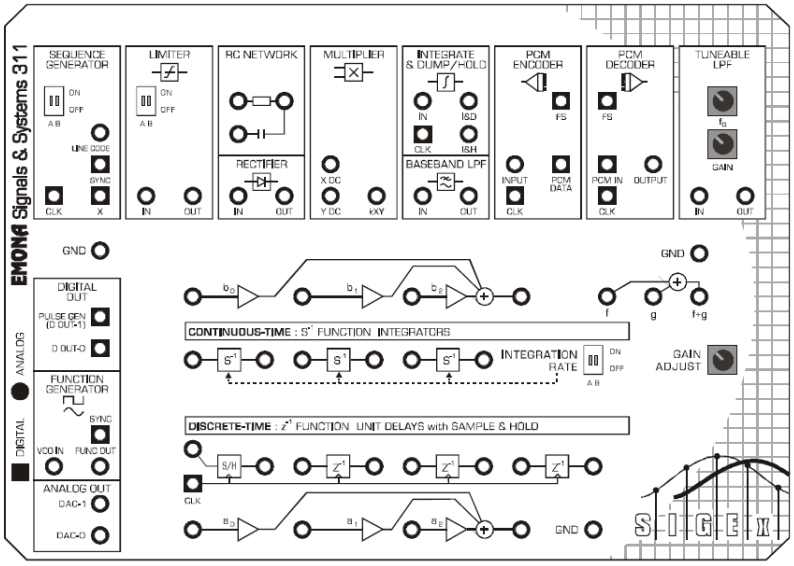


Figure 1-1 EMONA SIGEx board layout.

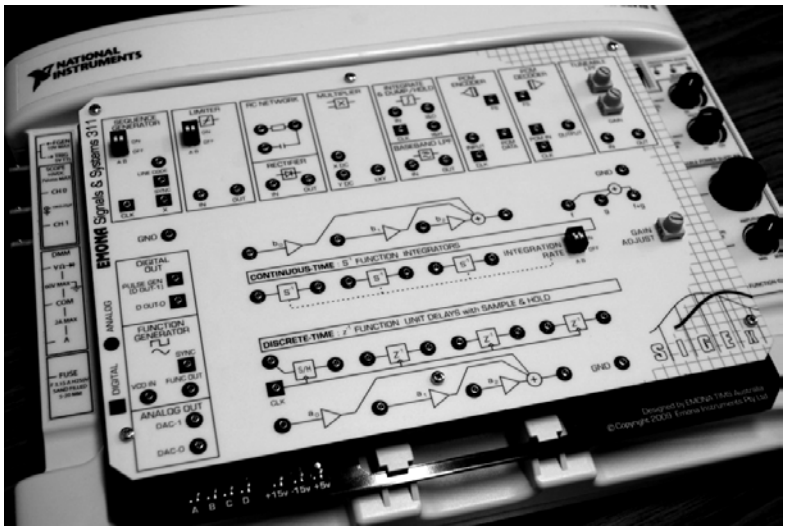


Figure 1-2 NI ELVIS II with EMONA SIGEx board.

EMONA SIGEx SET-UP

1. Turn off the NI ELVIS unit and its Prototyping Board switch.
2. Plug the SIGEx board into the NI ELVIS unit (this might have been done already).
3. Connect the NI ELVIS to the PC using the USB cable (if not connected already).
4. Turn on the PC (if not on already) and wait for it to fully boot up (so that it's ready to connect to external USB devices).
5. Turn on the NI ELVIS unit but not the Prototyping Board switch yet. You should observe the USB light turn on (top right corner of ELVIS unit).The PC may make a sound to indicate that the ELVIS unit has been detected if the speakers are activated.
6. Turn on the NI ELVIS Prototyping Board switch to power the SIGEx board. Check that all three power LEDs are on. If not call the instructor for assistance.
7. Launch the SIGEx Main VI.
8. When you're asked to select a device number, enter the number that corresponds with the NI ELVIS that you're using.
9. You're now ready to work with the NI ELVIS/SIGEx bundle.

Note: To stop the SIGEx VI when you've finished the experiment, it's preferable to use the STOP button on the SIGEx Soft Front Pannel (SFP) itself rather than the LabVIEW window STOP button at the top of the window. This will allow the program to conduct an orderly shutdown and close the various DAQmx channels it has opened.

PRELAB

1. Please go over Table 1-1 for a description of the functionality of the circuit modules contained in the SIGEx board.
2. Please go over Table 1-2 for a description of the functionality of NI ELVIS function blocks contained in the SIGEx board.
3. Identify the location of each circuit module and function block in the actual board and create a simplified diagram of the SIGEx board identifying the location of each module.

SIGEx Board Circuit Modules and NI ELVIS Function Blocks

Table 1-1 EMONA SIGEx circuit modules.

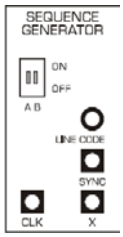
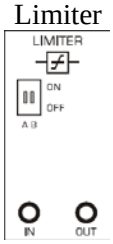
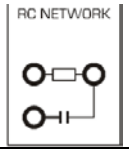
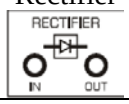
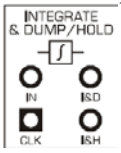
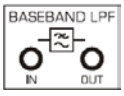
Sequence Generator 	The SEQUENCE GENERATOR provides a source of periodic data streams which are output as 5V logic and bipolar level signals. DIP switches allow the selection of 4 different streams. A periodic SYNC pulse is output once per frame. The module is clocked by a single input logic level clock. This will typically come from the PULSE GENERATOR or FUNCTION GENERATOR/SYNC outputs. The state of the DIP switches at any time is displayed on the SIGEx SFP along with a description.
Limiter 	The LIMITER amplifies an incoming signal with DIP switch selectable gain levels and to a fixed level, creating an amplitude limited output signal. It is typically used with bipolar analog sinusoidal signals or bipolar line coded data streams.
RC Network 	The RC NETWORK provides R and C elements which can be arranged as either an RC circuit which acts as a LPF, or as a HPF. The elements are floating and one end needs to be connected to GND.
Rectifier 	The Rectifier provides half wave rectification of an incoming signal with a non ideal diode component which has a forward voltage drop. This is typically used with sinusoidal signals.
Multiplier 	The Multiplier provides four quadrant multiplication of two analog input signals. Its overall gain is approximately unity and it is used to model any multiplication process that may occur in a block diagram.
Integrate & Dump/Hold 	Both Integrate and Dump as well as Integrate and Hold is available in this circuit block. Usually clocked by the bit clock of an incoming sequence, it is used to integrate over a single period of a waveform in correlation and filtering functions.
Baseband Low Pass Filter 	This LPF has a 4th order Butterworth response and serves both as a "system under investigation" and for general filtering functions.

Table 1-1 EMONA SIGEx circuit modules. Cont.

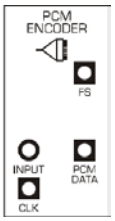
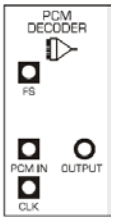
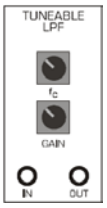
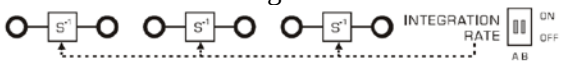
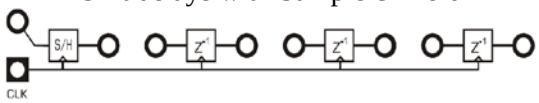
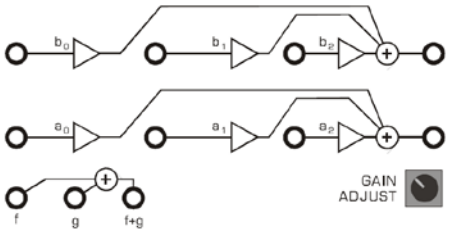
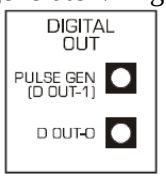
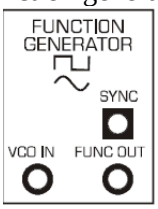
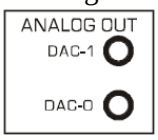
PCM Encoder 	This module implements PCM encoding of a single analog signal. It outputs an 8 bit frame along with a periodic Frame Sync pulse. It can be used with both DC signals as well as sinusoids and serves to allow specific investigation of the encoding process. It has a maximum sampling rate of 2.5ksps (20kbps PCM data stream), and so can be used with signal frequencies below the Nyquist limit of 1.25kHz.
PCM Decoder 	This module implements PCM decoding of an 8 bit PCM digital data stream from the PCM Encoder. The Frame Sync is necessary to achieve synchronization and there is no reconstruction filter on the output to allow investigation of quantization issues.
Tuneable Low Pass Filter 	This module is an adjustable LPF. It implements a 8th order Elliptic filter with an adjustable corner frequency. The output signal level is also adjustable, and it can accept analog and TTL level digital signals. There is no anti-aliasing filter on the input so users need to be aware of the bandwidth of their incoming signal.
Integrators 	These 3 independent circuits are simple integrator circuits with a common DIP-switch- selectable integration rate. They are used for continuous time integration (unlike the Integrate & Dump/Hold unit which operates over a single period only.) They are used in Laplace domain experiments. The DIP switch settings is displayed in the SIGEx SFP along with the approximate integration rate.
Unit delays with Sample & Hold 	The Sample & Hold is an analog sampler circuit which holds the sampled value for a single period of the incoming TTL level clock signal. The unit delays are similar in that they hold the incoming analog value at their input for a single clock period. All 4 units share a common clock signal.
Triple and dual input adders 	There are 3 adder sections. Two identical triple input adder sections and a dual input adder. The triple input adders, a & b, have adjustable gains. These gains are adjusted via the SIGEx SFP and are typically used to implement the taps in feedback and feedforward systems. The dual input adder has unity gain and is used for general purpose addition. The GAIN ADJUST knob is read by the SIGEx SFP software and can be used to manually adjust adder gains.

Table 1-2 NI ELVIS function blocks.

Pulse generator / Digital out 	This module makes available the built in Pulse Generator from NI ELVIS which has a very broad range of frequency and duty cycle control. This is controlled from the SIGEx SFP and is usually used to provide digital clock signals to experiments. D-OUT-0 is a single digital output line which is available but currently unused in experiments.
Function generator 	This module makes available the built in Function Generator from NI ELVIS which is a multifunction generator, with variable signal types, variable amplitude and variable frequency. It is controlled via its own instrument panel which available from the NI ELVIS Instrument Launcher panel
Analog out 	This module makes available the built in dual analog outputs from the DACs. These outputs are controlled from various SIGEx experiment TABs and can be modified to create any periodic waveforms required.

EMONA SIGEx Soft Front Panel (SFP)

When using NI ELVIS with the EMONA SIGEx board to conduct signals and systems experiments the students will run the SIGEx Main SFP VI shown in Figure 1-3 below. The SIGEx SFP serves both to control elements of the SIGEx hardware, as well as provide experiment specific measuring instrumentation. The layout is arranged so as to fit on screen easily with all parameters in view.

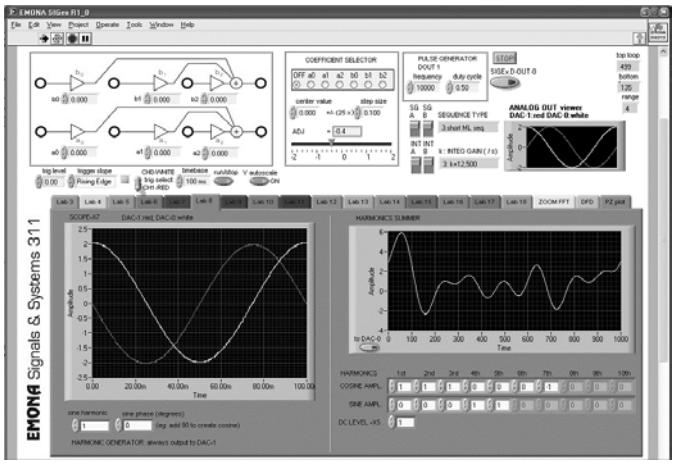


Figure 1-3 EMONA SIGEx Soft Front Panel.

These instruments take their signals directly from the SIGEx board into the ELVISmx circuitry, and after processing by LabVIEW are displayed on screen as required.

Soft Front Panel (SFP) Descriptions
This section discusses the functionality of the SIGEx SFP briefly.

1. Please go over the star menu and run the "SIGEx Rx_x.exe" to open the EMONA SIGEx Main SFP VI, a window similar to Figure 1-3 should open.
2. **Identify the ADDER Gain entry panel**. The triple input adders have variable gains which are set from the entry controls on the SFP. These gains can also be set programmatically as is done in several experiment TABS. The onscreen gains are transferred to the hardware automatically and continuously.
3. **Identify the Coefficient Selector panel.** The position of the onboard GAIN ADJUST knob can be interpreted as a range of values set to a particular adder gain control. The radio button panel is used to select a particular gain control, or none. The center value and step size of each increment from the GAIN ADJUST knob must also be set. This allows either a broad range of values or a narrow focused range of values to be adjustable via the knob.
4. **Identify the Pulse Generator panel.** In the panel the frequency and duty cycle of the PULSE GENERATOR block can be set. As well the spare D-OUT-0 line can be toggled.
5. **Identify the SG Sequence type and Integrator Gain readouts.** These readouts mimic the selection of the onboard DIP switches and the text briefly describes the signal type selected for convenience.
6. **Identify the Analog OUT viewer.** This graph indicator displays the actual signal currently being output from the ANALOG OUT terminals from the DACs. These vary depending on the experiment selected, and this readout is convenient when SCOPE channels are being used for other signals.
7. **Identify the SCOPE Trig level, trigger slope, triggered LED, trig select, timebase etc.** These controls are for the SFP scopes embedded in various experiment TABs. Trig level sets the voltage level the trigger looks for. Usually set to 0 or 1 V Trig slope allows triggering on either the positive or negative edge of a signal. Triggered LED is ON (green) when a trigger point, as defined above, is detected. Trig select determines which channel acts as the trigger. Timebase varies the amount of real signal time to be captured and displayed. Total time displayed is selectable.
8. **Identify the RUN/STOP.** It enables halting of the scope display for close inspection.
9. **Identify the Y autoscale ON.** It enables toggling of the Y axis autoscale function for stable signal viewing with varying amplitude signals.
10. **Identify the Laboratory Experiment 'X' TABS**. Each experiment may use one or more Laboratory Experiment TAB. Select the TAB as required and the appropriate instrumentation will be displayed.

HINT: Right-clicking on a graph will display extra available options you can use. Different options are available when you right-click while the SFP is not running eg: setting a graph from linear to log display is done while SFP is not running.

11. **Select the Digital Filter Design (DFD) TAB**. This TAB makes available several of the digital filter design features from the toolkit in one handy display. The user should select a filter type from which the transfer function will be calculated. The coefficients from the transfer function are extracted and setup on the SIGEx hardware as the triple ADDER gains when required by the user. This can be seen on the SFP. The calculated responses are displayed onscreen.

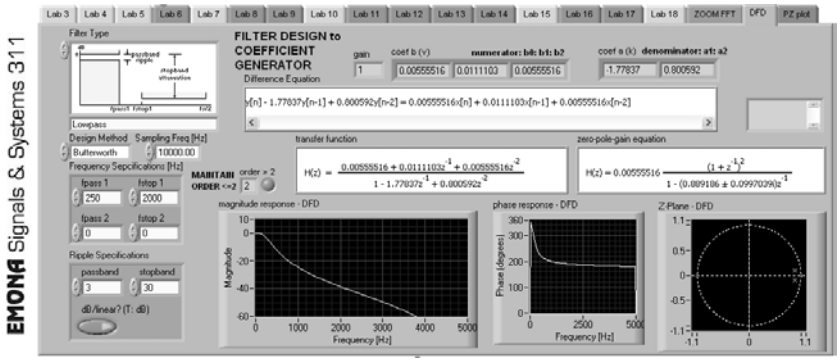


Figure 1-4 Digital Filter Design Tab.

12. **Select the ZOOM FFT TAB. This** TAB contains a scope display, a spectrum display, and a zoomable view of the FFT display. This TAB is a general purpose display TAB and is not associated with any particular experiment. The FFT display is a 1000 point display, and the "# samples" control allows the user to select a zoom window from 0 to 1000 points to display alongside. The "zoom region" slider enables the zoom region to be selected from the overall 1000 point FFT display.

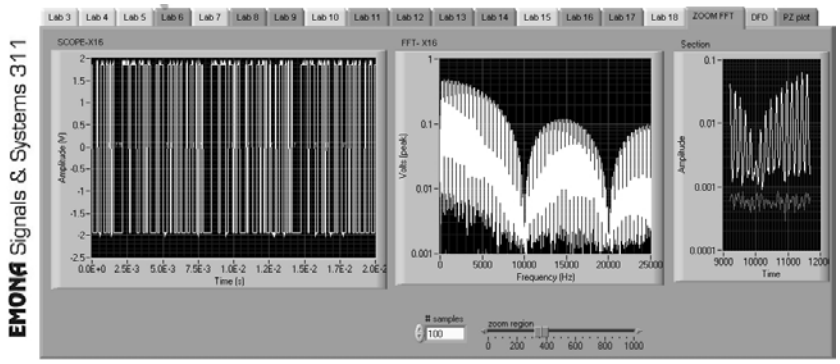


Figure 1-5 Zoom FFT Tab.

13. **Select the PZ PLOT TAB.** This TAB calculates and plot the poles and zeros on the unit circle from the coefficients of the transfer function as it is set up on the SIGEx board. The coefficient values from the triple ADDER gain controls are read by this TAB and plotted as the equivalent poles and zeros in real time. This is especially interesting when the coefficients are being varied manually by the onboard GAIN ADJUST knob, in that the user can see the poles and zeros moving about the unit circle in real time alongside the hardware.

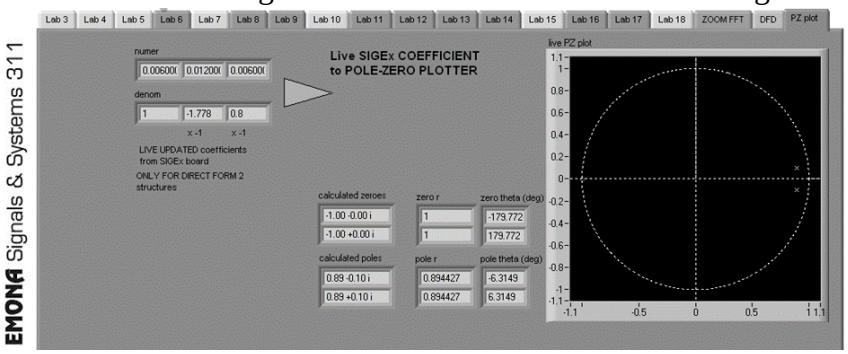


Figure 1-6 PZ PLOT Tab.

PROCEDURE

Sinewave Input

Sinewaves are encountered in a large number of applications. In this experiment the students will carry out some basic observations and compare the sinewave response of the various Systems Under Investigation (SUI).

1. Connect the FUNC OUT output from the FUNCTION GENERATOR to the inputs of the systems under investigation (See Figure 1-7).
2. Launch the NI ELVIS Intrument Launcher and select the FUNCTION GENERATOR. Set up the FUNCTION GENERATOR as follows:
   a. Select: SINE wave
   b. Voltage range: 4V pp
   c. Frequency: 100 Hz
   d. Press RUN when ready.
3. Connect CH0 of the scope to the output of the FUNCTION GENERATOR, and CH1 to the output of the systems under investigation (one at a time)
   a. Baseband LPF
   b. Tunable LPF
   c. RC Network
4. Progressively increase the frequency from 100 Hz to 10 kHz and observe the effect on the amplitude of the output signal. Make a record of your findings in Table 1-3.
5. Enter your results into the table on the TAB3 SIGEX application, which will plot those results. Consider the possible advantage of using log scales. To enable a “log” Y axis, stop the SIGEX SFP program, right click the plot graph, select Visible Items > Scale Legend then select the third button to the right of Amplitude, select Mapping Mode > Logarithmic. To return to Linear, repeat this process and select “Linear”.
6. Save the resulting plot.

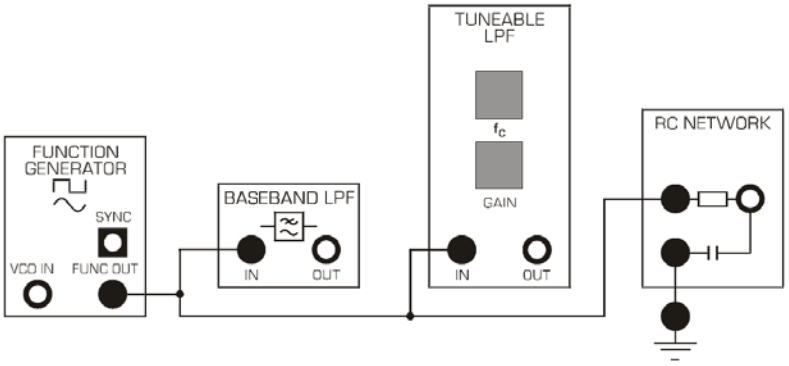


Figure 1-7 Patching Diagram for Sinewave Input.

Voltage Limiter

A common example of voltage clipping or limiting occurs in amplifiers when the signal amplitude is too high for the available DC supply voltage headroom. In audio systems clipping is undesirable as it causes distortion of the sound. However, in other applications, a clipped signal can be useful. Here we examine the operation of the voltage LIMITER.

1. Connect the system in Figure 1-8.
2. Since we will be using the MEDIUM mode of the LIMITER unit, the on-board switches must be set accordingly (swA= OFF, swB= OFF).
3. Tune the FUNCTION GENERATOR to 1200Hz and select SINUSOIDAL output with 4 Vpp.
4. Set scope as follows:
   a. SCOPE: Timebase 2ms;
   b. Rising edge trigger on CH0;
   c. Trigger level=0V
5. Display the output and input of the LIMITER, and observe the effect of changing the amplitude at the AMPLITUDE control of the FUNCTION GENERATOR. Make it larger and smaller.
6. Record your output voltage (Vpp) vs input voltage (Vpp) findings in Table 1-4.

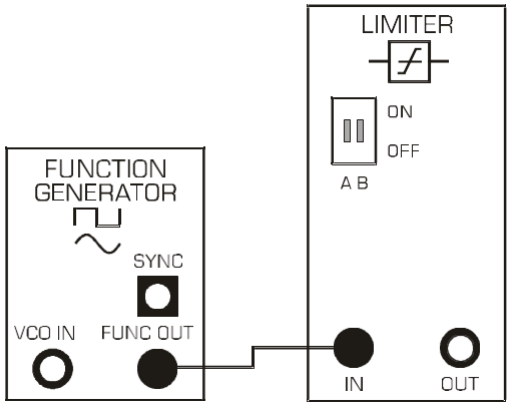


Figure 1-8 Patching Diagram for Voltage Limiter.

DATA/OBSERVATIONS

Table 1-3 Amplitude vs Frequency for Sinewave Input

Frequency (Hz)	BLPF (Vpp)	TLPF (Vpp)	RCLPF (Vpp)

INSTRUCTOR'S INITIALS: | | DATE: | |

Table 1-4 Output Voltage vs. Input Voltage for Limiter Circuit

Input (Vpp)	Output (Vpp)

INSTRUCTOR'S INITIALS: DATE:

POST-LAB

Post-Lab questions must be answered in each experiment's laboratory report. Ask your Lab TA about any preferences on how to incorporate this information into the report.

1. Plot the data collected in Table 1-3. Discuss/compare the results and observations from the three systems under investigation.
2. Plot the data collected in Table 1-4. Discuss the results and obesrvations for the voltage limiter circuit.