UNIVERSITY OF NORTH CAROLINA AT CHARLOTTE
Department of Electrical and Computer Engineering

EXPERIMENT 5 – ZENER DIODE VOLTAGE REGULATOR, DIODE CLIPPERS AND CLAMPERS

OBJECTIVES

The purpose of this experiment is to investigate the application of a Zener diode for voltage regulation and also diode applications in clipping and clamping circuits.

INTRODUCTION

In Figure 5-1, an often used Zener diode voltage regulator is shown. The function of a voltage regulator is to provide a constant low ripple output voltage under varying load current conditions. While very high quality voltage regulators are available in integrated circuits, at times it may be sufficient and convenient to use a simple Zener diode regulator. Since the Zener diode will conduct in the reverse direction for any V_o greater than V_z, V_o can never exceed V_z. As the load current changes the Zener diode will conduct sufficient current to maintain a voltage drop of $E - V_o$ across the series dropping resistor, R_s.

The selected Zener diode must have a reverse breakdown voltage equal to the desired output voltage and be capable of dissipating the power that results when R_L is very large. This type of regulator is generally not good for output voltages less than 5 volts or so because low voltage diodes with a sharp knee at reverse breakdown are not available. The difference between E and V_o should be selected as small as possible but must be large enough to prevent the voltage drop across R_s from exceeding $E - V_o$, when I_L is maximum. It is clear that a smaller value for R_s translate to a smaller value for $E - V_o$; however, a smaller value for R_s will result in a greater diode current when R_L is large and this will increase the power dissipation requirement of the diode.

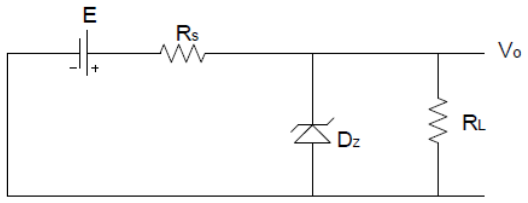


Figure 5-1 Zener Diode Voltage Regulator

Often in the development of electronic circuits it is required that voltages be limited in some manner to avoid circuit damage. Furthermore, the limiting or clipping of voltages can be very useful in the development of wave-shaping circuits. A typical clipper circuit is shown in Figure 5-2. In this circuit the output voltage can never be greater than 3V. The ideal diode becomes forward biased at V_o equal to 3V and this ties the output directly to the 3V supply. The

waveform can be clipped on the negative side by placing the series combination of a diode and power supply in parallel with the diode and power supply already shown.

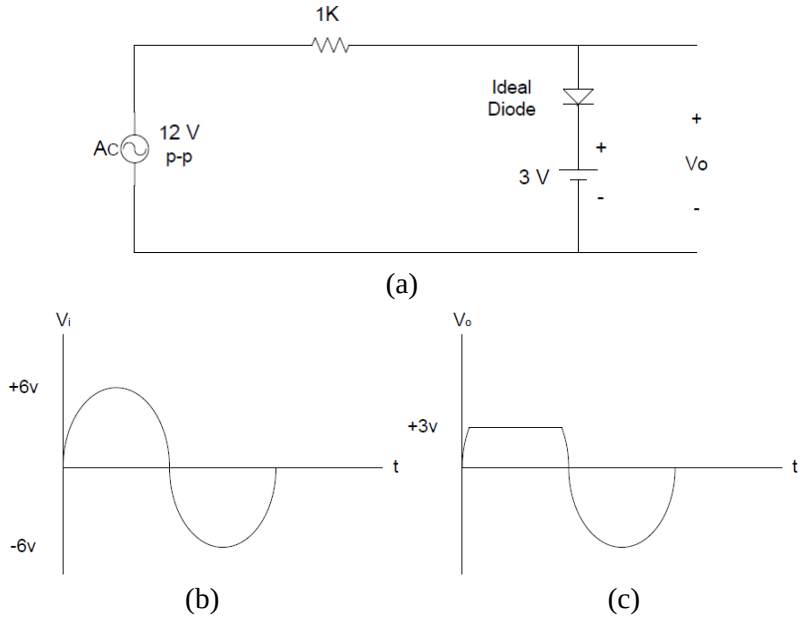


Figure 5-2 (a) Diode Clipper Circuit, (b) Input Voltage, (c) Output Voltage

While clipper circuits are concerned primarily with limiting or cutting off part of the waveform, clampers are used primarily to shift the DC level. For example, if we have a clock signal that swings between 0V and 5V but our application requires a clock signal from -5V to 0V, we can provide the proper DC offset with a passive clamper circuit. A typical clamper circuit is shown in Figure 5-3. For this circuit to work properly the pulse width needs to be much less than the RC time constant of 10 ms. The input square wave with a frequency of 1 kHz and a pulse width of 0.5 ms meets this requirement. The diode and power supply as shown will prevent the output voltage from exceeding 3V (i.e., all of the region above 3 V can be viewed as a forbidden region for output voltage).

Because of the time constant requirement the voltage across the capacitor cannot change significantly during the pulse width, and after a short transient period the voltage across the capacitor reached a steady state offset value. The output voltage is simply the input voltage shifted by this steady state offset. Also, observe that the peak-to-peat output voltage is equal to the peak-to-peak input voltage. This is true because the voltage across the capacitor cannot change instantaneously and the full change of voltage on the input side of the capacitor will likewise be seen on the output side of the capacitor.

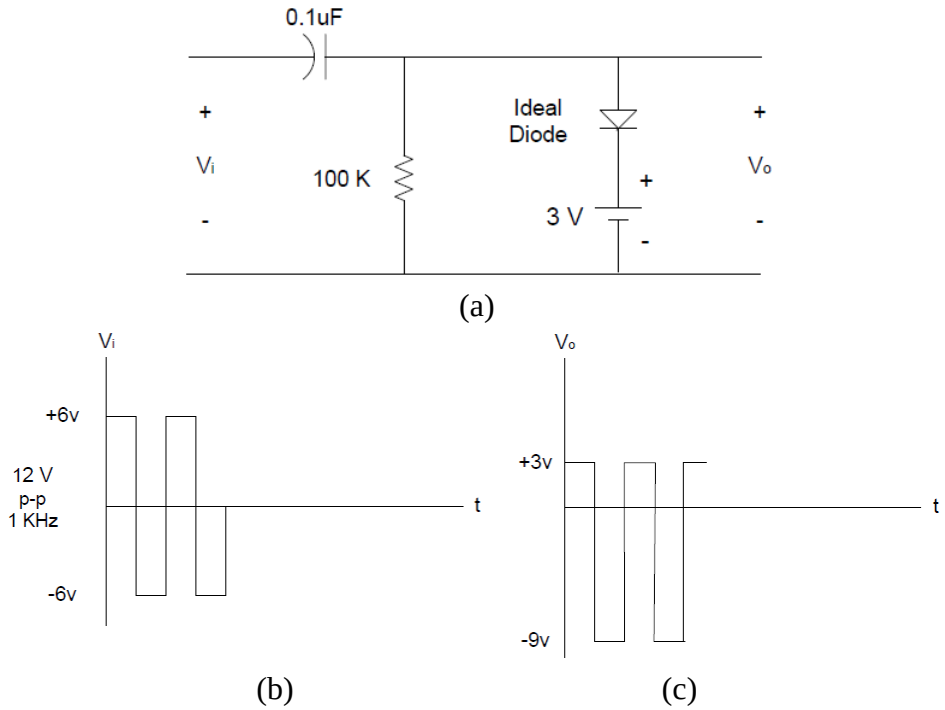
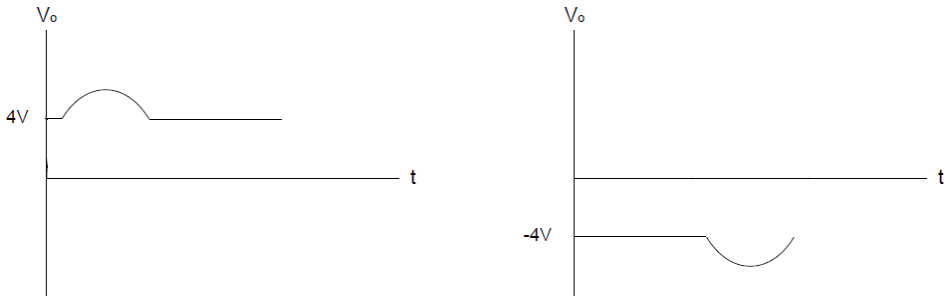


Figure 5-3 (a) Diode Clamper Circuit, (b) Input Voltage, (c) Output Voltage

PRELAB

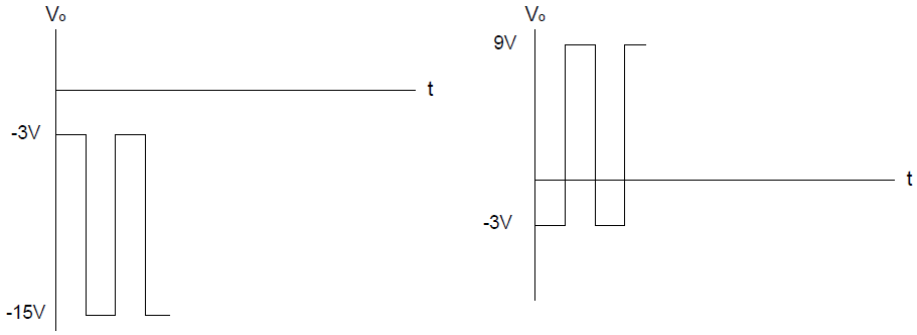
1. Assume that you have a 20 V DC power supply with a voltage regulation of nearly 100%, and a 5 % peak-to-peak 60 Hz ripple at its full load current of 5 mA. You wish to build a Zener diode regulated power supply, as shown in Figure 5-1, with a 13 V DC output and a maximum load current of 5 mA. Determine the largest possible value for R_s, and the Zener breakdown voltage and power rating.
2. Show the circuit diagrams for clipper circuits, similar to the circuit of Figure 5-2, which will provide the clipped output waveforms as shown in (a) and (b) of Figure 5-4. Assume a sinusoidal input voltage with a peat-to-peak value of 12 V.



(a) (b)

Figure 5-4 Clipper Outputs for Prelab Question #2

3. Show the circuit diagrams for clamper circuits, similar to the circuit of Figure 5-3, which will provide the clamped output waveforms in (a) and (b) of Figure 5-5



(a) (b)

Figure 5-5 Clamper Outputs for Prelab Question #3

NOTE: During the experiment you will need a means of saving waveforms measured with the oscilloscope in order to perform the experiment and answer the post-lab questions.

PROCEDURE

1. Construct the voltage regulator circuit designed in part #1 of the Pre-lab. Verify its operation by observing the output voltage on the oscilloscope while the load resistor is changed to provide load currents of 5 mA, 2.5 mA, and 0.0 mA.
2. Measure and record the peak-to-peak ripple in the output for the 5 mA load current. This will require use of the most sensitive voltage scale and AC coupling.
3. Using a DC current meter to measure the load current, select a load resistor that will provide a load current of 10 mA. Record the DC output voltage.
4. Construct and verify operation of the clipper circuit in Figure 5-2, and those designed in part #2 of the Pre-lab.
5. The output waveforms should be observed on the oscilloscope in the DC coupling mode. Save your waveforms.
6. Construct and verify operation of the clamper circuit in Figure 5-3, and those designed in part #3 of the Pre-lab.
7. The output waveforms should be observed on the oscilloscope in the DC coupling mode. Save your waveforms.

POSTLAB

Post-Lab questions must be answered in each experiment's laboratory report.

1. We know that the output ripple voltage of the regulator constructed in step #1 of the Procedure is not absolutely zero. If it was impossible to observe an output ripple, explain what caused this limitation. Explain why the output voltage drops below its design value when the maximum load current is exceeded.
2. Did the clipper circuits in step 4 of the Procedure work as expected? Include your recorded waveforms in the lab report. Explain the effects of using a diode that is not ideal. Under what circumstances would the effects of a non-zero forward resistance and a non-zero knee voltage be most observable?
3. Did the clipper circuits in step 6 of the Procedure work as expected? Include your recorded waveforms in the lab report. Explain what happens when the pulse with is not much less than the circuit time constant. Determine how long it will take for the DC offset seen in the output to reach its final value. What complications would you anticipate when using this type of circuit to drive a low impedance clock input?