Control Number:_____

Department of Electrical and Computer Engineering

Fall 2023 COMPREHENSIVE/BREADTH EXAM

Questions 2/3/4 | TTG Area: Devices Circuits & Systems | ECGR-4146: Introduction to VHDL

Question 2) Short Question answers

1) What does "Read First" mean in the context of memory?? **(2 points)**
   a) Simultaneously read the current value and update
   b) Read the new value after update
   c) Read the current value and update the signal later
   d) Only read and no write

2) The output of the sequential circuit is regarded as a function of the time sequence of_____.
   (2 points)

   1.Variables
   2. Outputs
   3. States
   4. External inputs

   a) 4 and 1
   b) 1 and 3
   c) 1 and 2
   d) 3 and 4

3) The FSMD routing circuit in the datapath is constructed by customized _____ **.**
   (Hint : The circuit routes the source registers' outputs to the proper functional units and routes the calculated results from the functional units to proper destination registers using the state_reg as control signal) **(2 points)**
   a) Adders
   b) Subtractors
   c) Multiplexers

4) What is the difference between the Moore machine and the Mealy machine? Discuss the design tradeoffs with respect to performance and area overheads.

Points breakdown:

a) Difference between Moore machine and Mealy machine:**2 points**
b) Performance in terms of clock cycles and no. of states :**3 points**

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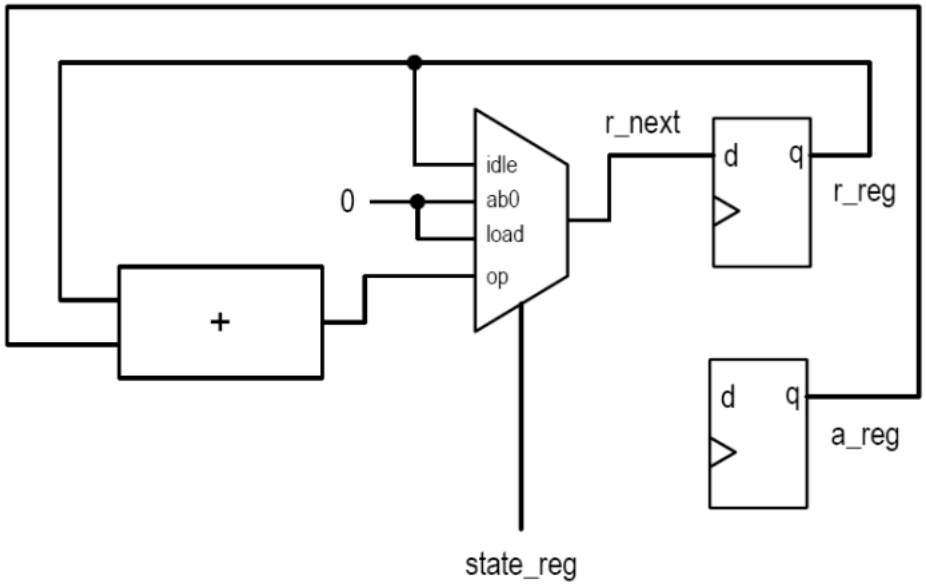
Question 3) Write the VHDL instructions for register a and r ?



Entity

Architecture

Begin

Process( )

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Question 4) For the following branch predictor, assume the initial state is s0. Design the ASM chart for the following state machine.
No VHDL code is required.