

Department of Electrical and Computer Engineering
COMPREHENSIVE/BREADTH EXAM

Questions 2/3/4

TTG Area: Devices Circuits &
Systems

ECGR-4146: Introduction to VHDL

Question 2) Short Question answers

a)

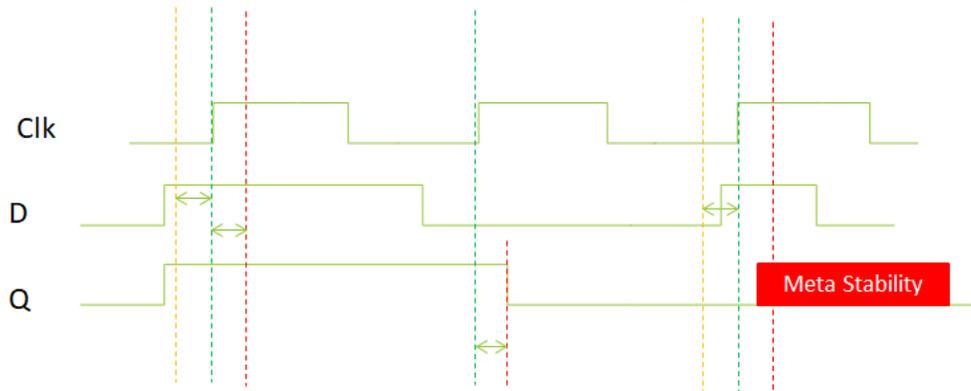
```

library ieee;
use ieee.std_logic_1164.all;
entity Example_demo is
port(
  a, b: in std_logic;
  x, y: out std_logic);
end mode_demo;
architecture arch of Example _demo is
begin
  x <= a not b;
  y <= not x;
end arch;

```

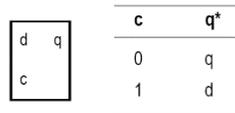
Identify the mistake and correct the design.

b) For the given timing waveform, show and discuss the timing parameters for a D-Flipflop.

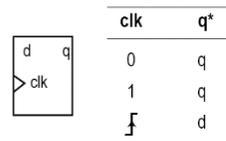


c) Define CLB, explain the generic configuration of CLB for Xilinx architectures.

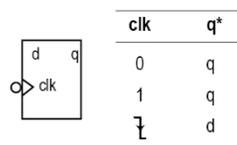
d) Write a behavioral VHDL description for the following memory elements.



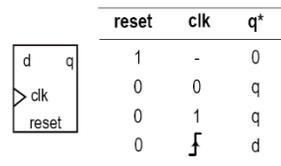
(a) D latch



(b) pos-edge triggered D FF

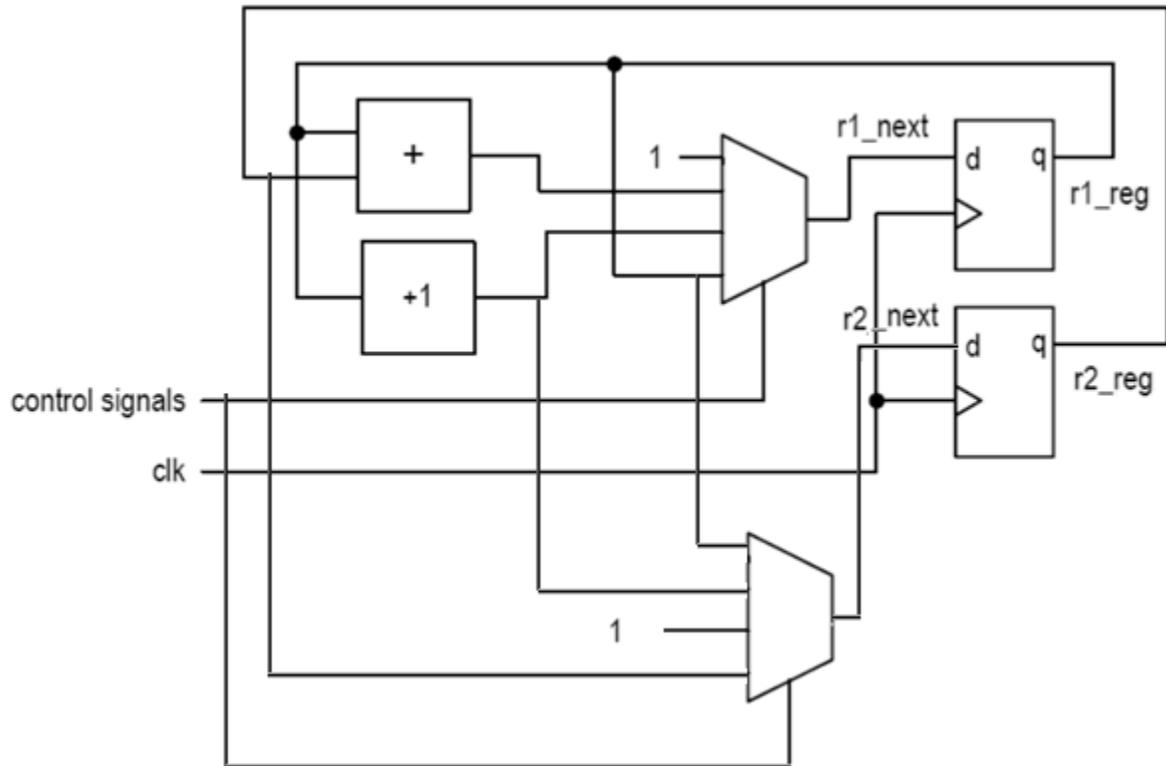


(c) neg-edge triggered D FF



(d) D FF with asynchronous reset

Question 3) Write the VHDL code for the following block diagram



Entity

Architecture

Begin

Process()

Question 4) Design a regular sequential circuit of a counter that counts from 1 -1000. An initial value from data input is loaded on the counter register when the load signal is enabled.

```
library ieee;
use ieee.std_logic_1164.all ;
use ieee.Numeric_std.all ;
entity COUNTER is
generic ( WIDTH : in natural := 32);
port ( RST : in std_logic;
        CLK : in std_logic;
        LOAD : in std_logic;
        DATA : in std_logic_vector(WIDTH-1 downto 0);
        Q : out std_logic_vector(WIDTH-1 downto 0));
end entity COUNTER;
);
end reg_file;

architecture
```